

10/502099

FIG. 1A

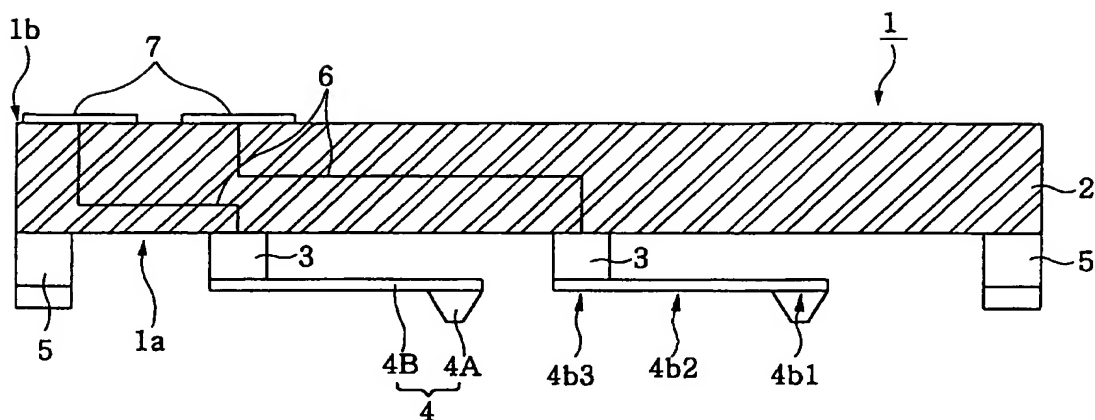
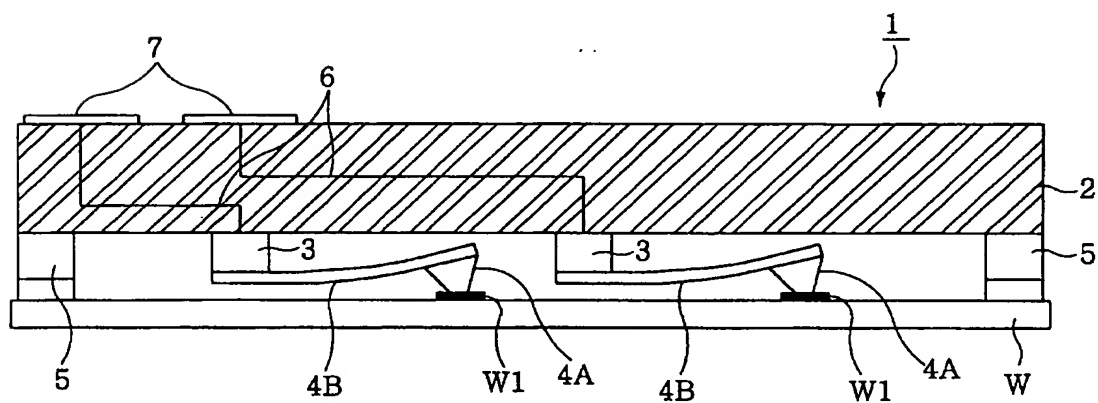


FIG. 1B



10/502099

FIG. 2A

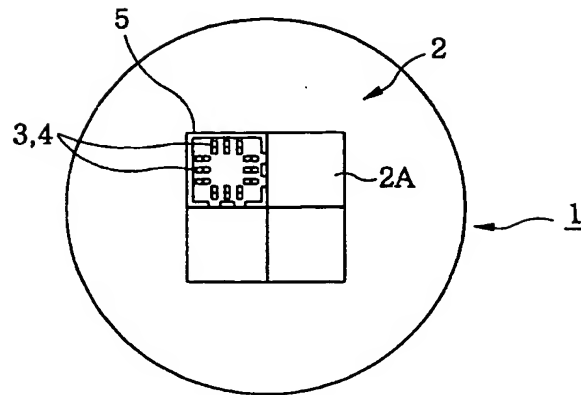


FIG. 2B

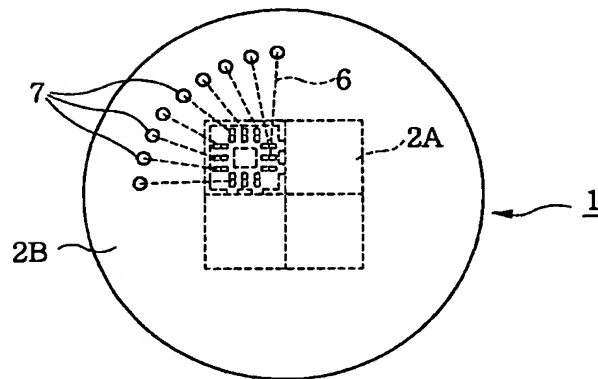
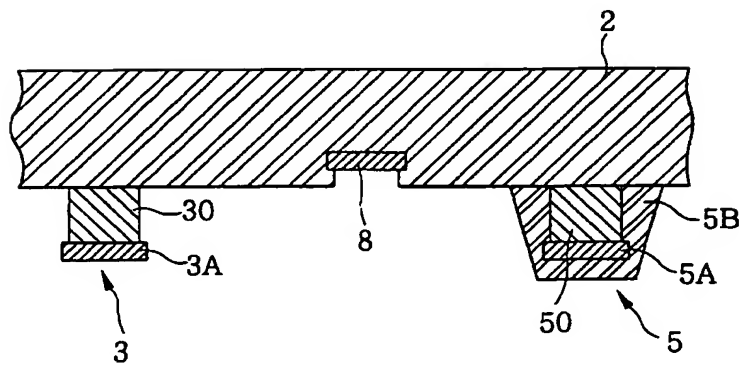
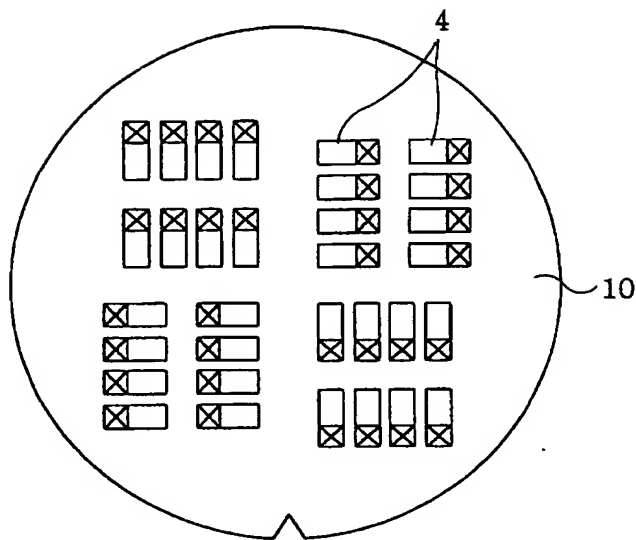
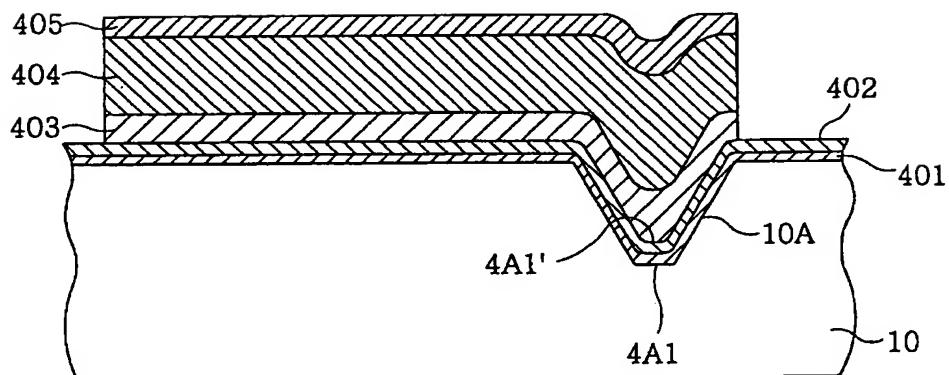


FIG. 3



10/502099

FIG. 4A**FIG. 4B**

10/502099

FIG. 5A

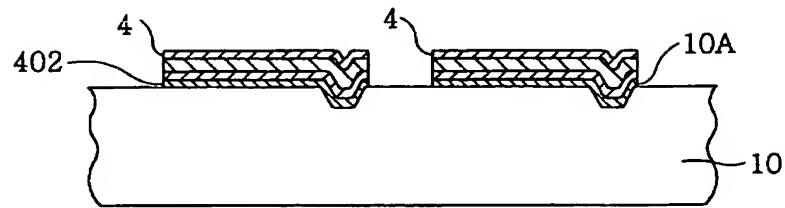


FIG. 5B

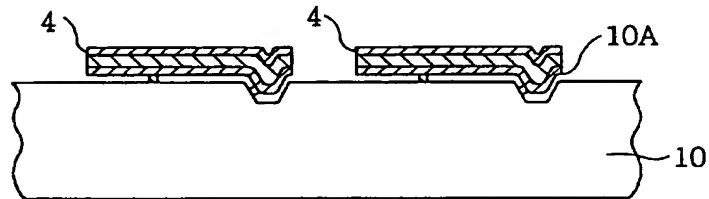
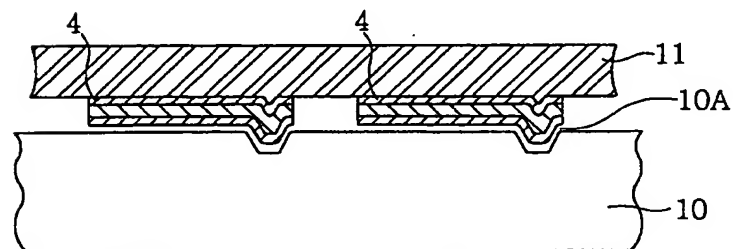


FIG. 5C



10/502099

FIG. 5D

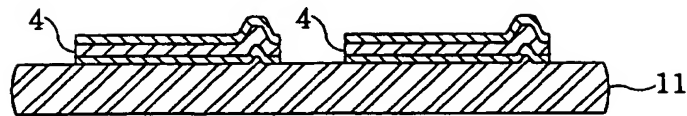


FIG. 5E

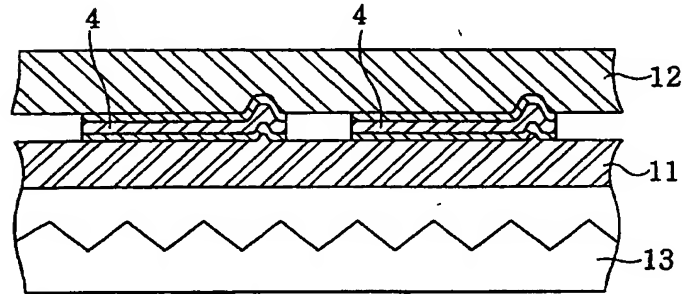


FIG. 5F

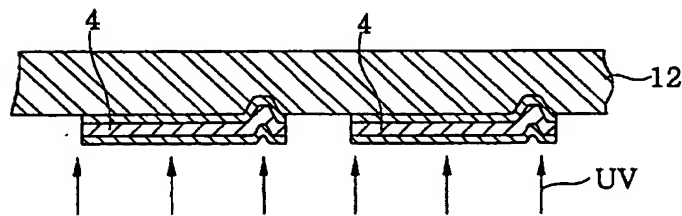


FIG. 5G

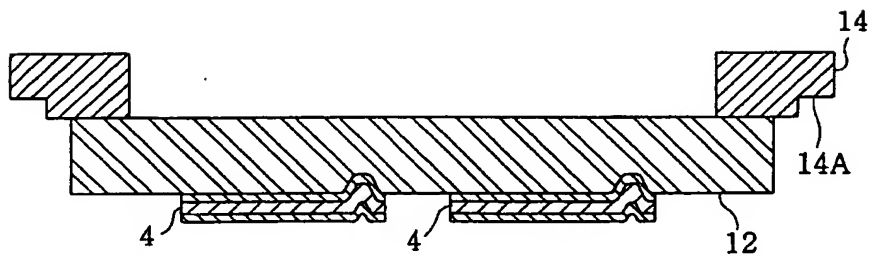
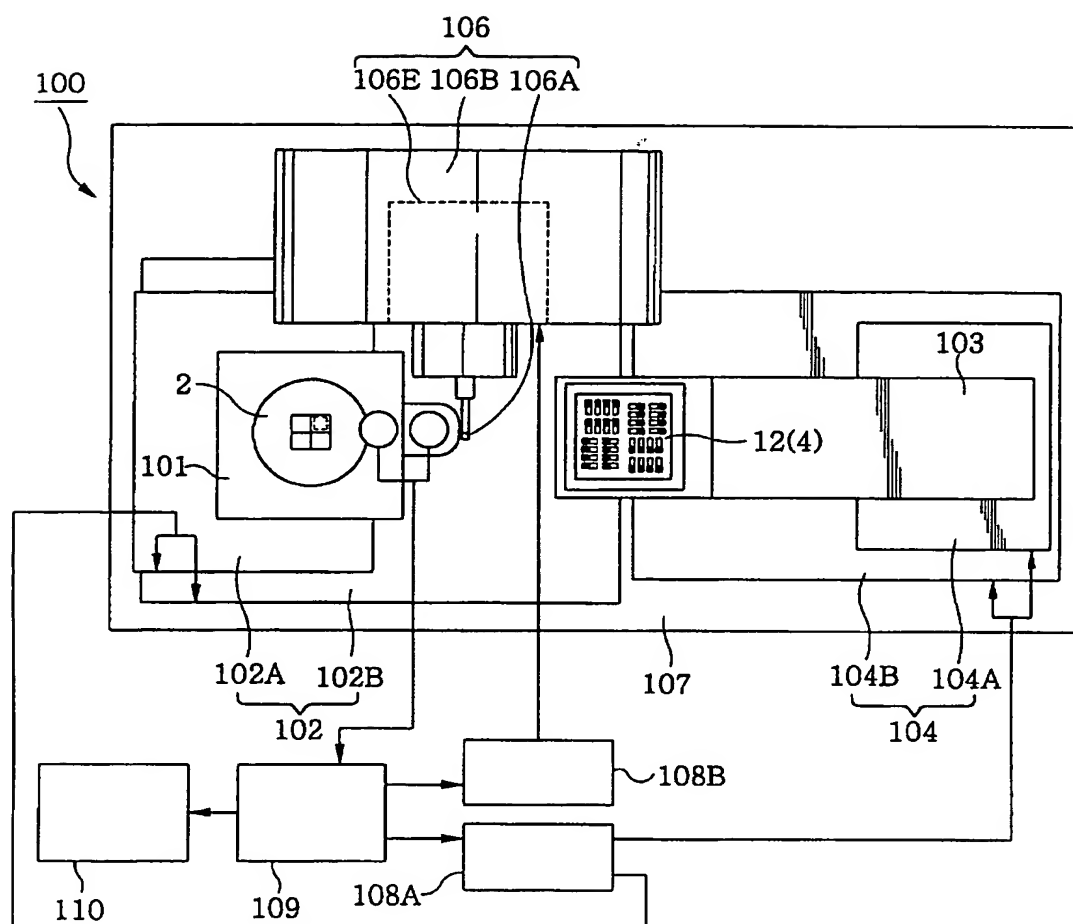


FIG. 7



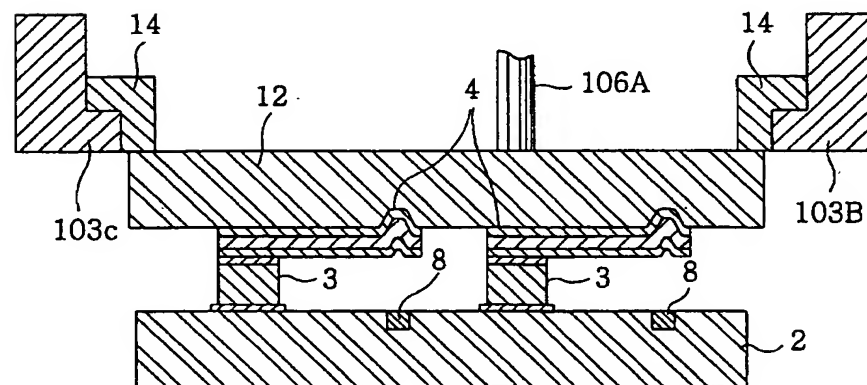


FIG. 8D

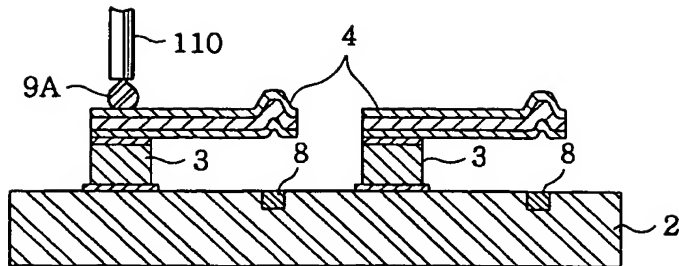


FIG. 8E

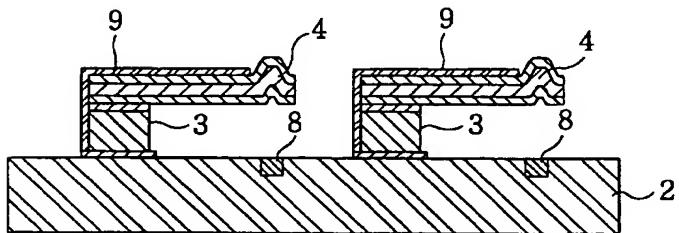


FIG. 9

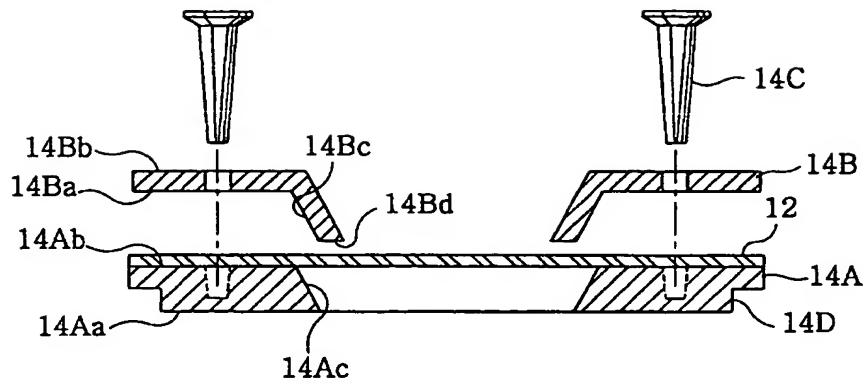


FIG. 10

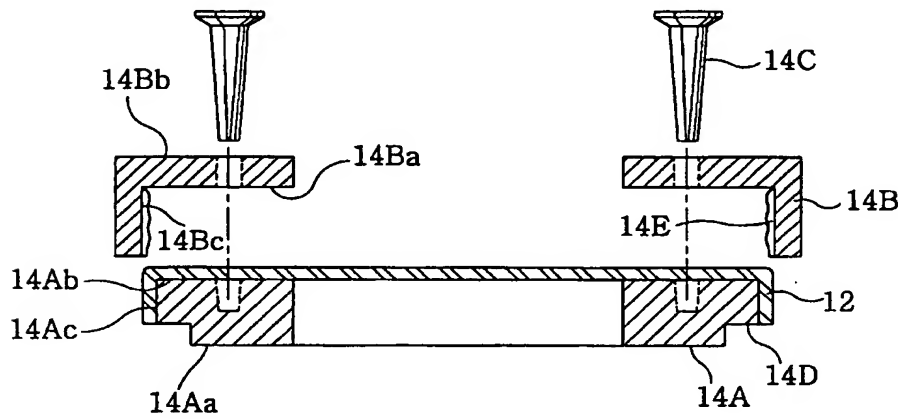


FIG. 11

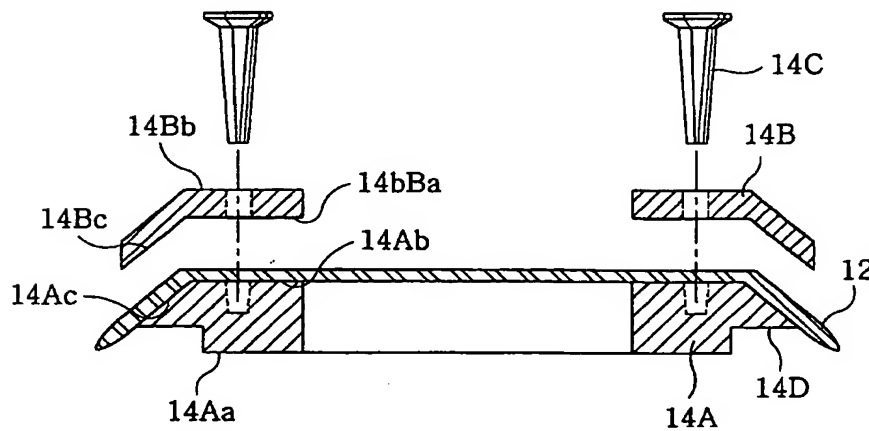
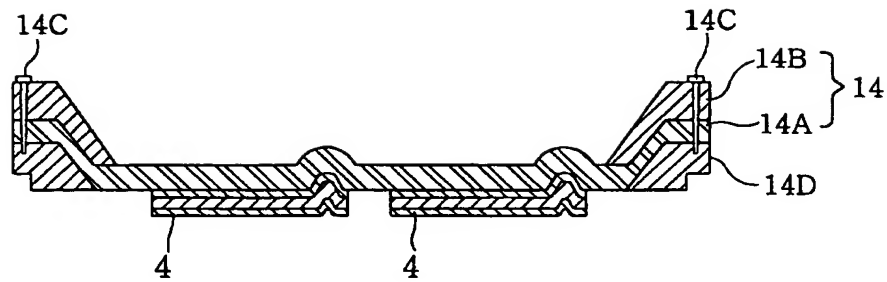


FIG. 12



This cross-sectional view shows a semiconductor device. A substrate 2 is at the bottom. On top of the substrate, there are gate stacks 3. Each gate stack 3 consists of a gate electrode 106A and a gate insulating layer 8. A gate 4 is formed on top of the gate stacks. A gate insulating layer 12 is formed on top of the gate. A gate electrode 14 is formed on top of the gate insulating layer 12. A gate insulating layer 103B is formed on top of the gate electrode 14. The gate insulating layer 103B is also formed on the substrate 2.

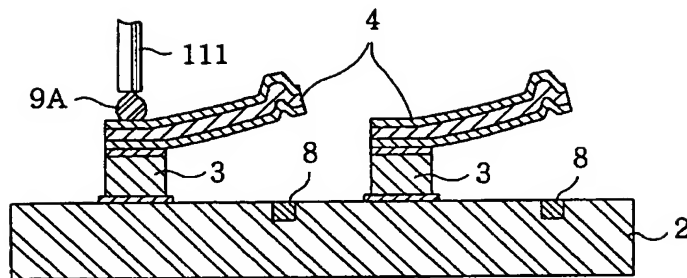
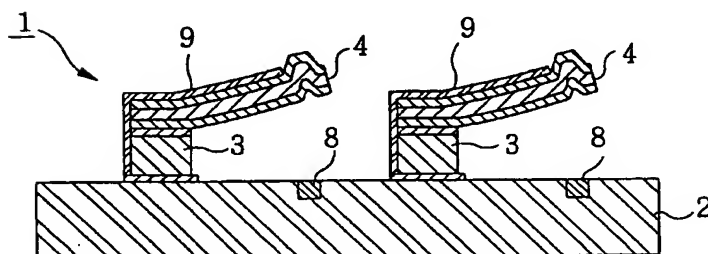
FIG. 13C**FIG. 13D**

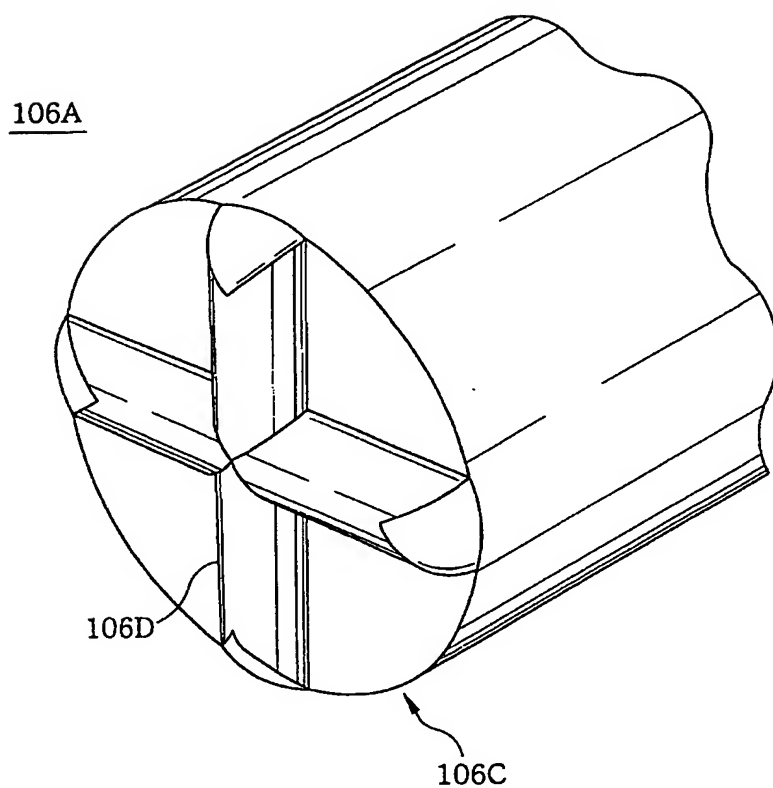
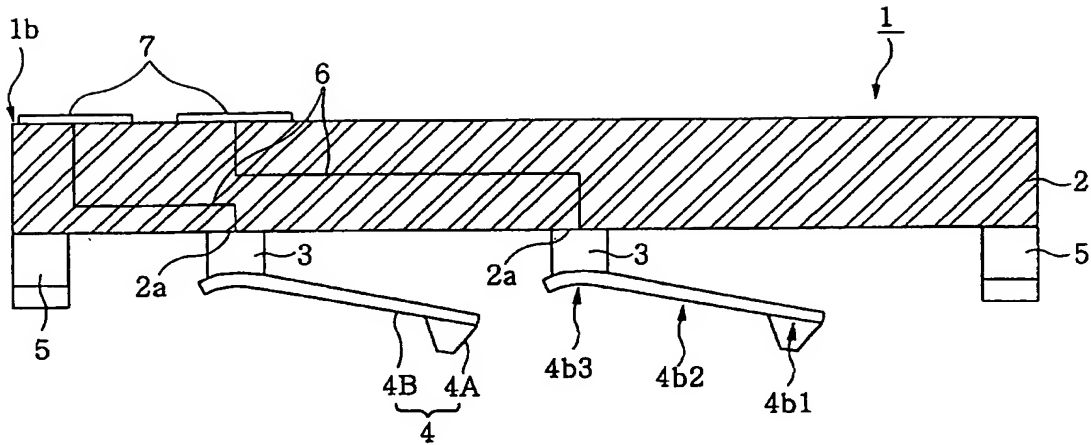
FIG. 14

FIG. 15A**FIG. 15B**